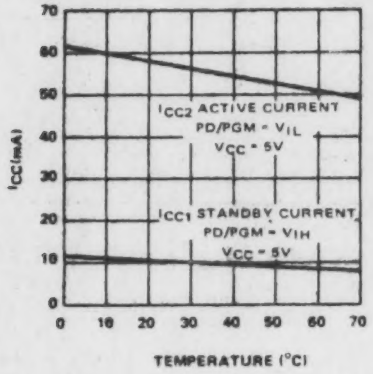
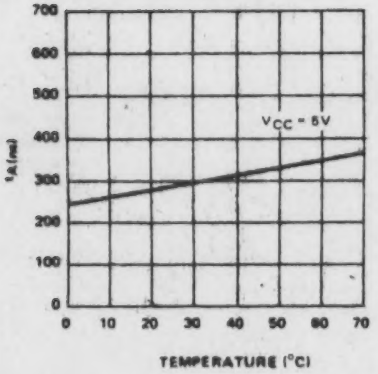
device characteristics (read mode)

TMS 2516-35
I_{CC} CURRENT
vs
TEMPERATURE



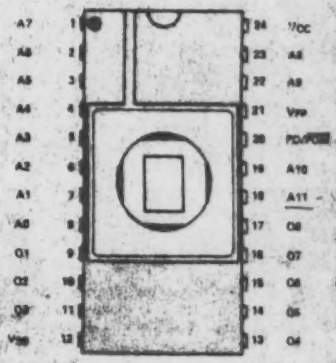
TMS 2516-35
ACCESS TIME
vs
TEMPERATURE



2532

- Organization . . . 4K X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- 40% Lower Power
  TMS 25L32 . . . 500 mW Max Active
  TMS 2532 . . . 840 mW Max Active
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

TMS 2532
24-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
PD/PGM	Power Down/Program
O(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 25L32 JL is a 32,768-bit, low-power ultraviolet-light-erasable, electrically programmable read-only memory. This device is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS 25L32 is plug-in compatible with the TMS 4732 32K ROM. It is offered in a dual-in-line ceramic sidebraze package (JDL suffix) rated for operation from 0°C to 70°C.

Since this EPROM operates from a single +5 V supply (in the read mode), it is ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

ion

FUNCTION (PINS)	MODE				
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming
PGM (20)	V_{IL}	V_{IH}	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH}
	+5 V	+5 V	+5 V	+25 V	+25 V
	+5 V	+5 V	+5 V	+5 V	+5 V
o 11, o 17)	Q	HI Z	HI Z	D	HI Z

read/output disable

When the outputs of two or more TMS 25L32's are connected on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the PD/$\overline{PGM}$ pin. All other devices in the circuit should have their outputs disabled by applying a high-level signal to this pin. Output data is accessed at pins Q1 through Q8. Data can be accessed in 450 ns = $t_{a(A)}$.

power down

Active power dissipation can be cut by over 70% by applying a high TTL signal to the PD/$\overline{PGM}$ pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 25L32 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state (assuming high-level output corresponds to logic "1").

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when Vpp is 25 V. Data is presented in parallel (8 bits) in pins Q1 through Q8. Once addresses and data are stable, a 50-millisecond TTL low-level pulse should be applied to the $\overline{PGM}$ pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. Several TMS 25L32's can be programmed simultaneously when the devices are connected in parallel.

inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen TMS 25L32's not intended to be programmed should have a high level applied to PD/$\overline{PGM}$.

program verification

The TMS 25L32 program verification is simply the read operation, which can be performed as soon as Vpp re +5 V ending the program cycle.

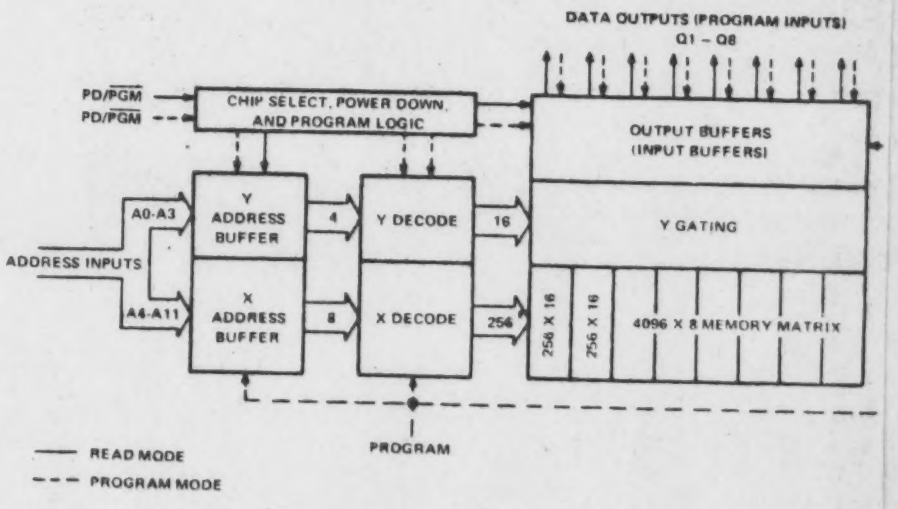
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0
Supply voltage, Vpp (see Note 1) . . . . . –0.3
All input voltages (see Note 1) . . . . . –0.
Output voltage (operating with respect to V_{SS}) . . . . . –0.
Operating free-air temperature range . . . . . 0°C
Storage temperature range . . . . . –55°C t

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Co section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device r

functional block diagram



ndad operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
ltage, V_{CC} (see Note 2)	4.75	5	5.25	V
ltage, V_{PP} (see Note 3)	V_{CC}–0.6	V_{CC}	V_{CC}+0.6	V
ltage, V_{SS}		0		V
input voltage, V_{IH}	2.0		V_{CC}+1	V
Input voltage, V_{IL}	–0.1		0.8	V
e time, $t_{c(rd)}$	450			ns
free-air temperature, T_A	0		70	°C

V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} is applied.

V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. Tolerance of ± 6 volts enables the V_{PP} pin to be switched from V_{CC} (read) to 25 volts (programming) using a drive circuit. During programming, V_{PP} must be maintained at 25 V (± 1V).

characteristics over full ranges of recommended operating conditions

ARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
High-level output voltage	I_{OH} = –400 µA	2.4			V
Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
Input current (leakage)	V_I = 5.25 V			10	µA
Output current (leakage)	V_O = 5.25 V			10	µA
V_{PP} supply current	V_{PP} = 5.85 V, PD/$\overline{PGM}$ = V_{IL}			12	mA
V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		10	25	mA
V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		65	95	mA

ues are at T_A = 25°C and nominal voltages.

ice over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz

AMETER	TEST CONDITIONS	TYP†	MAX	UNIT
put capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
utput capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

values are T_A = 25°C and nominal voltage

switching characteristics over full ranges of recommended operating conditions, (unless otherwise noted)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, t_r≤20 ns, t_f≤20 ns		280	450	ns
$t_{a(PR)}$	Access time from PD/PGM			280	450	ns
t_{PVX}	Output not valid from address change		0			ns
t_{PXZ}	Output disable time from PD/PGM		0		100	ns

†All typical values are at T_A = 25°C and nominal voltages.

recommended timing requirements for programming T_A = 25°C (see Note 4)

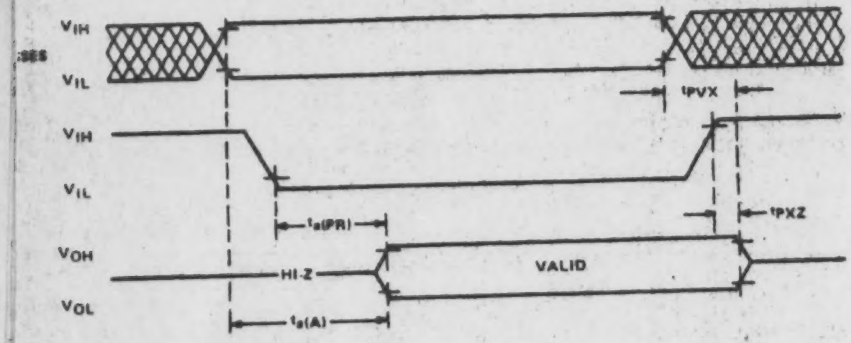
PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	Setup time from Vpp	0			ns
$t_{h(A)}$	Address hold time	2			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	Vpp hold time	0			ns

†Typical values are at nominal voltages.

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{PP} = 25 V ± 1 V during programming.

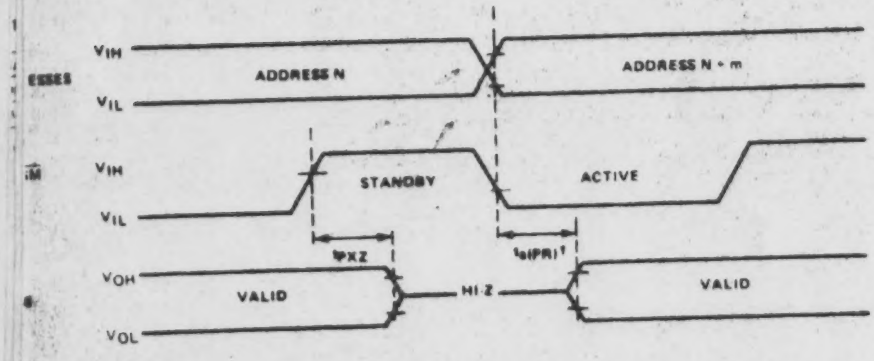
5. Common test conditions apply for t_{PXZ} except during programming. For $t_{a(A)}$ and t_{PXZ}, PD/$\overline{PGM}$ = V_{IL}.

le timing



There is no chip select pin on the TMS 25L32.
The chip select function is incorporated in the power down mode.

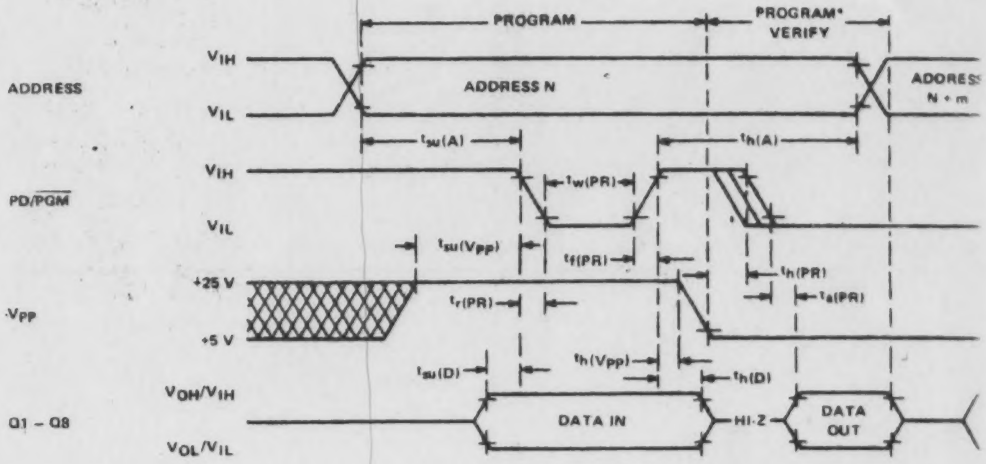
mode



†(a) referenced to PD/PGM or the address, whichever occurs last.

ing reference points in this data sheet (inputs and outputs) are 90% points.

program cycle timing



*Program verify equivalent to read mode.

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